**CPE 343 – Computer Organization & Architecture**

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**Lab # 3**

**Title: Design the combinational circuit using library building technique od VHDL programming.**

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| Name | Abdul Basit |
| Registration Number | FA17-BCE-062 |
| Class | FA17-BCE-B |
| Instructor’s Name | Moazzam Ali Sahi |

**INTRODUCTION:**

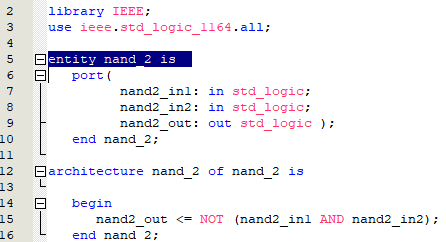
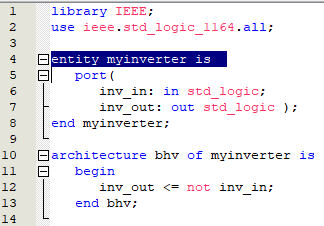
VHDL programming is used for parallel programing so in this lab we distributed our code into more than one VHDL file and created the package which contain different components and then we are going to link it with one main code.

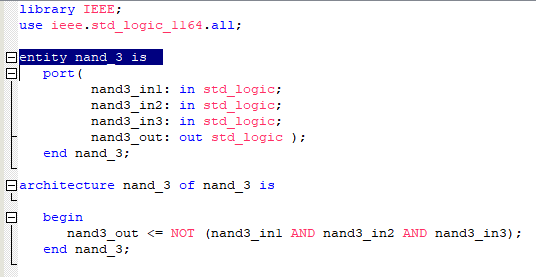
**LAB TASKS: (In-Lab Tasks)**

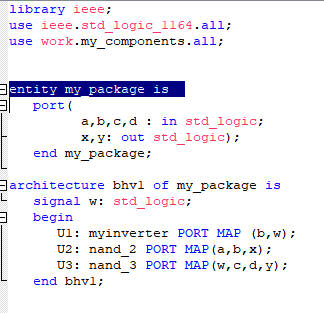
Implementation of inverter, nand with 2 input and nand with three input, into three vhdl cfile and use then by port mapping in the package file.

**Task 1:**

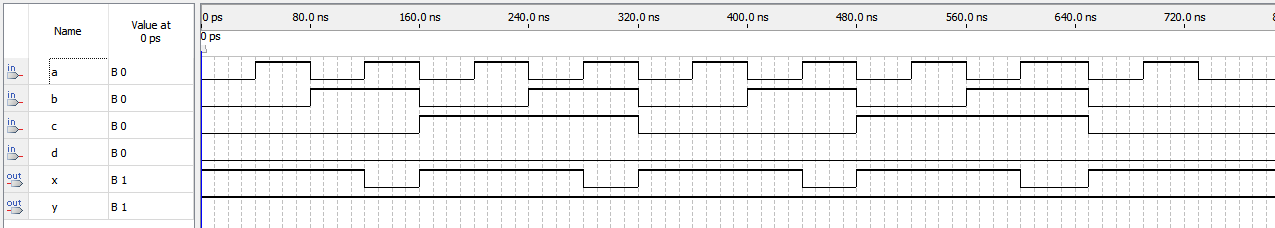
1. VHDL Code





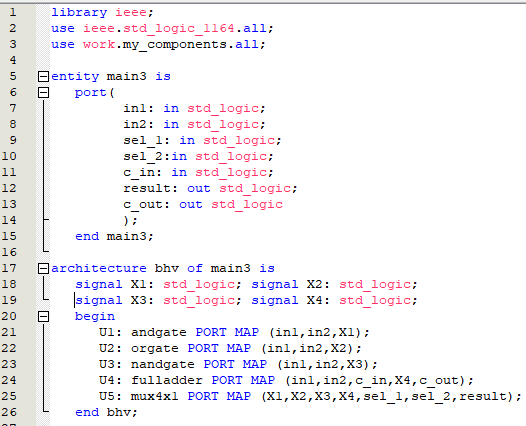


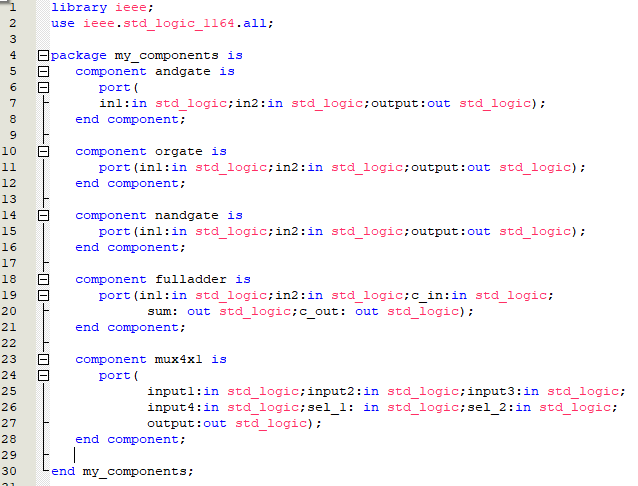
1. Results (VWF)

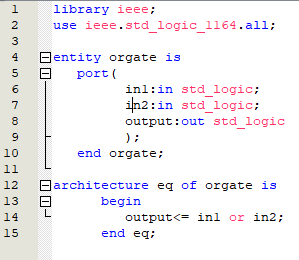
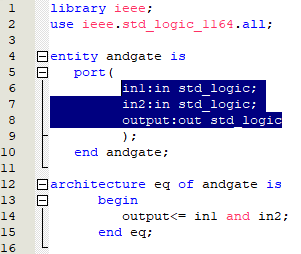


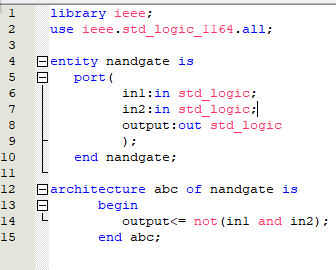
**Task 2:**

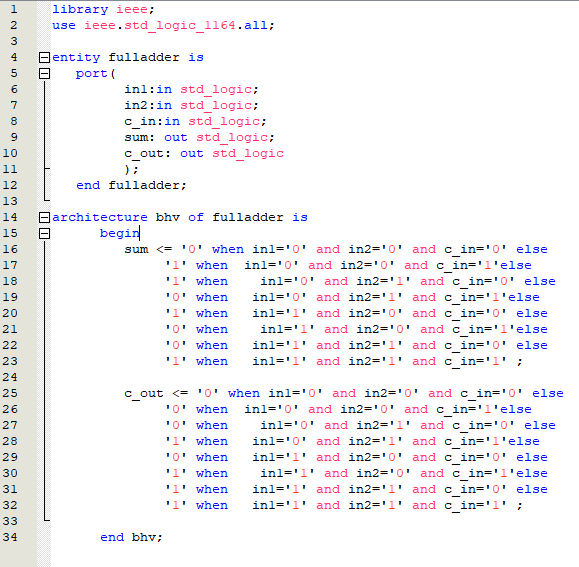
1. VHDL Code

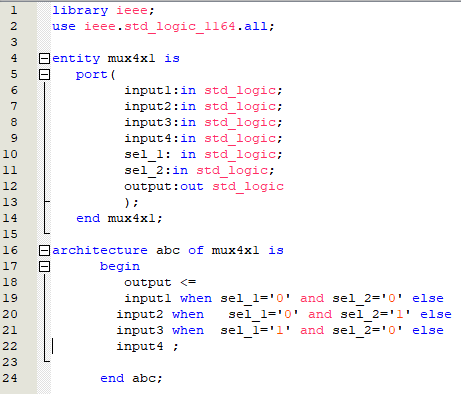




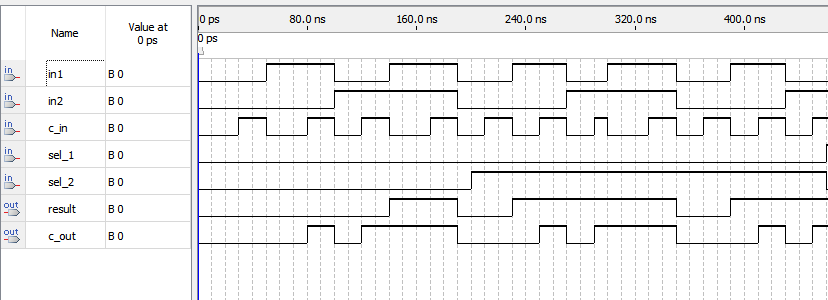








1. Results (VWF)



# CONCLUSION:

In this lab I learned how to use functions and components in Quatus II.And implemented 1 bit ALU.